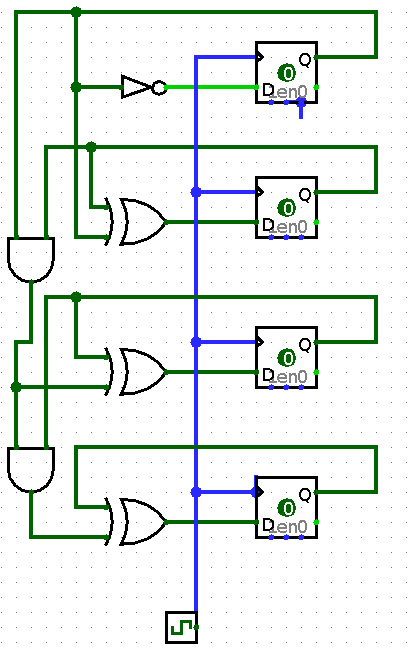
**Four Bit Counter**

1.



**2.** This module was designed to count from 0 to 15. The counter was implemented using registers and we incremented the value of the counter on the positive edge of every clock tick. The moment the counter hit 15, we reset it back to zero.

**3.**

===

\*.v

===

`timescale 1ns / 1ps

module my4BitCounter(rst,a,clk);

input clk;

input rst;

output reg [3:0] a;

always @ (posedge clk)

if (rst)

a <= 4'b0000;

else

a <= a + 1'b1;

endmodule

====

\*TB.v

====

`timescale 1ns / 1ps

`include "my4BitCounter.v"

module my4BitCounter\_TB;

// Inputs

reg rst;

reg clk;

// Outputs

wire[3:0] a;

// Instantiate the Unit Under Test (UUT)

my4BitCounter uut (.rst(rst), .a(a),.clk(clk));

initial begin

// Initialize Inputs

rst = 1'b1;

clk = 1'b0;

#2 rst = 1'b0;

end

initial

#200 $finish;

always

#1 clk = ~clk;

endmodule

====

\*.ucf

====

## Clock signal

NET "clk" LOC = "V10" | IOSTANDARD = "LVCMOS33"; #Bank = 2, pin name = IO\_L30N\_GCLK0\_USERCCLK, Sch name = GCLK

Net "clk" TNM\_NET = sys\_clk\_pin;

TIMESPEC TS\_sys\_clk\_pin = PERIOD sys\_clk\_pin 100000 kHz;

## Leds

NET "a<0>" LOC = "U16" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L2P\_CMPCLK, Sch name = LD0

NET "a<1>" LOC = "V16" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L2N\_CMPMOSI, Sch name = LD1

NET "a<2>" LOC = "U15" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L5P, Sch name = LD2

NET "a<3>" LOC = "V15" | IOSTANDARD = "LVCMOS33"; #Bank = 2, Pin name = IO\_L5N, Sch name = LD3

## Buttons

NET "rst" LOC = "B8" | IOSTANDARD = "LVCMOS33"; #Bank = 0, Pin name = IO\_L33P, Sch name = BTNS

**4.**

========================

Advanced HDL Synthesis Report

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Macro Statistics

# Counters : 1

4-bit up counter : 1

# Adders/Subtractors : 1

4-bit adder : 1

# Registers : 1

4-bit register : 1

# Registers : 4

Flip-Flops : 4

========================================

\* Design Summary \*

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Top Level Output File Name : my4BitCounter.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 4

# INV : 1

# LUT2 : 1

# LUT3 : 1

# LUT4 : 1

# FlipFlops/Latches : 4

# FDR : 4

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 5

# IBUF : 1

# OBUF : 4

Device utilization summary:

---------------------------

Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers: 4 out of 18224 0%

Number of Slice LUTs: 4 out of 9112 0%

Number used as Logic: 4 out of 9112 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 8

Number with an unused Flip Flop: 4 out of 8 50%

Number with an unused LUT: 4 out of 8 50%

Number of fully used LUT-FF pairs: 0 out of 8 0%

Number of unique control sets: 1

IO Utilization:

Number of IOs: 6

Number of bonded IOBs: 6 out of 232 2%

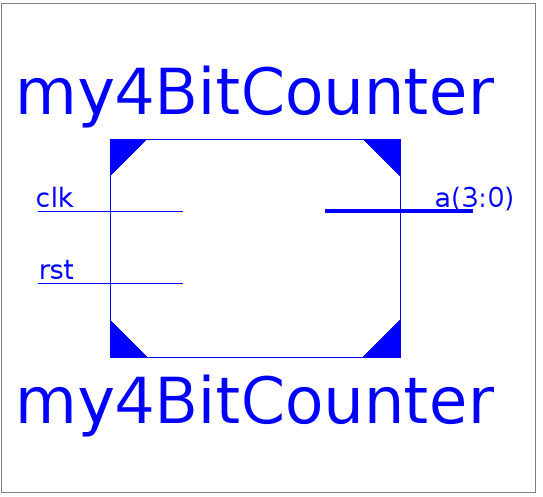
Specific Feature Utilization:

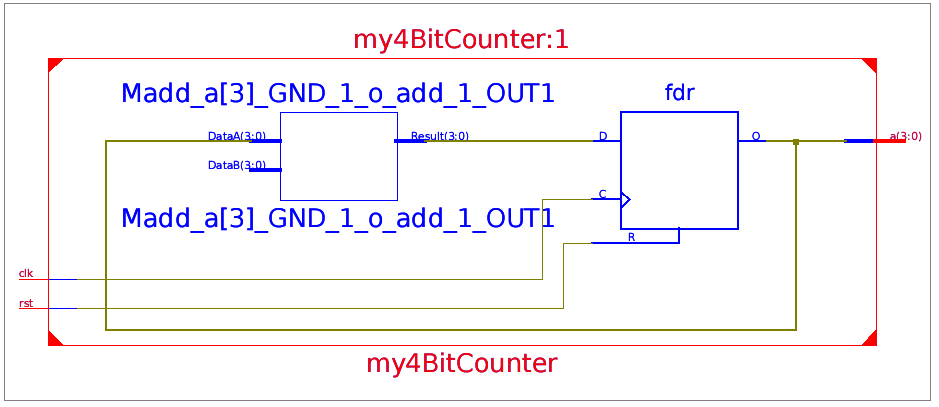
Number of BUFG/BUFGCTRLs: 1 out of 16 6%

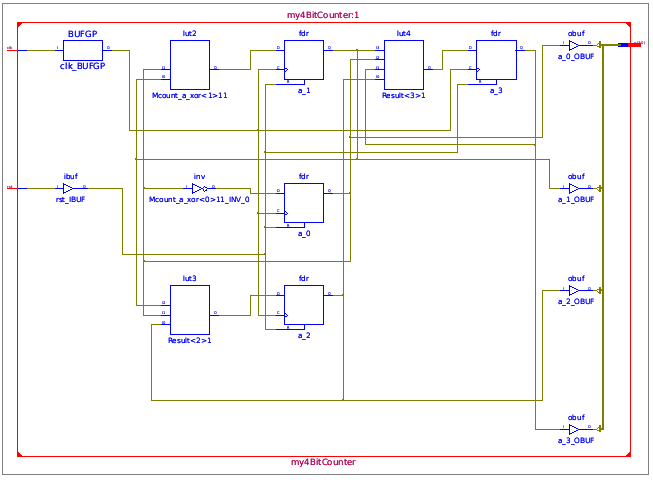
**5. Device Utilization Summary**

|  |  |  |  |
| --- | --- | --- | --- |
| Slice Logic Utilization | Used | Available | Utilization |
| # of Slice Registers | 4 | 19,224 | 1% |
| # used as Flip Flops | 4 |  |  |
| # of Slice LUTs | 4 | 9,112 | 1% |
| # used as logic | 4 | 9,112 | 1% |
| # using O6 output only | 4 |  |  |
| # of occupied Slices | 1 | 2,278 | 1% |
| # of LUT Flip Flop pairs used | 4 |  |  |
| # of fully used LUT-FF pair | 4 | 4 | 100% |
| # of unique control sets | 1 |  |  |
| # of slice register sites lost to control set restrictions | 4 | 18,224 | 1% |
| # of bonded IOBs | 6 | 232 | 2% |
| # of LOCed IOBs | 6 | 6 | 100% |
| # of BUFG/BUFGMUXs | 1 | 16 | 6% |
| # used as BUFGs | 1 |  |  |
| Avg Fanout of Non-Clock Net | 3.17 |  |  |

**6. High Level Schematic**







**7. Max Clock Frequency:** 578.035MHz

**8. Waveform**

